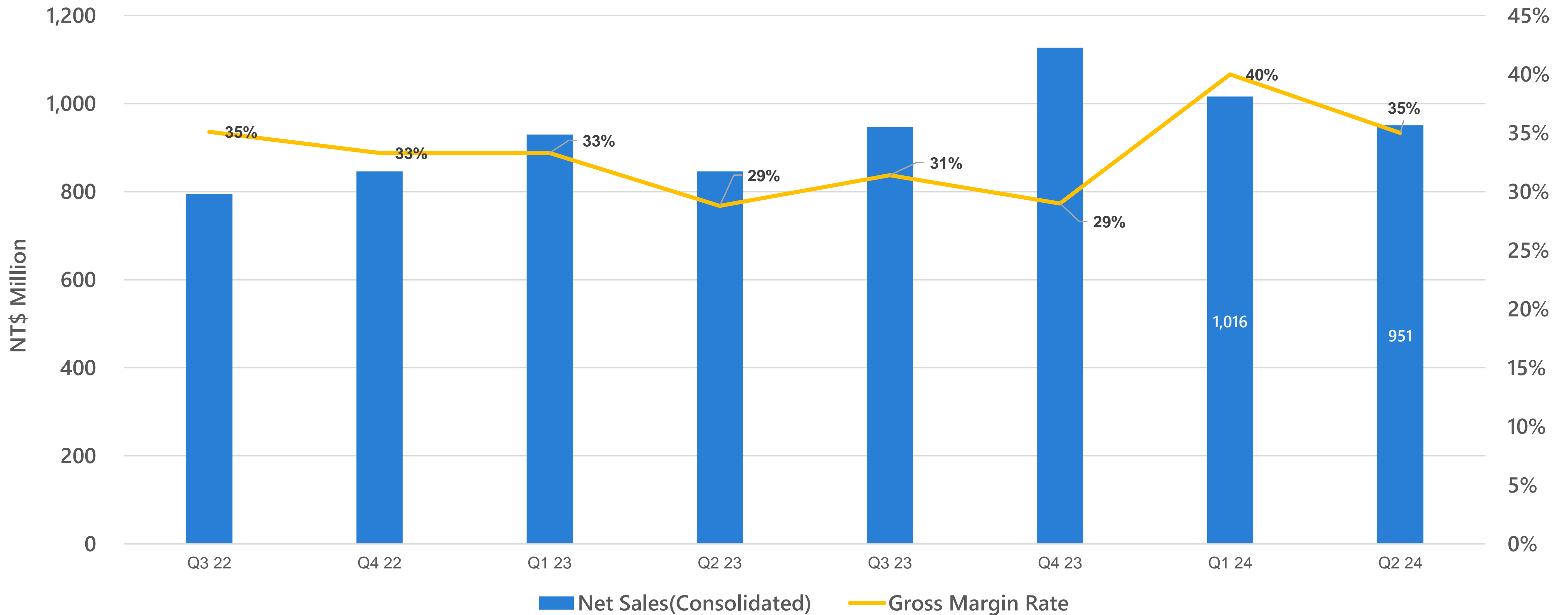
Egis Technology Inc.

2024Q2 Investor Conference

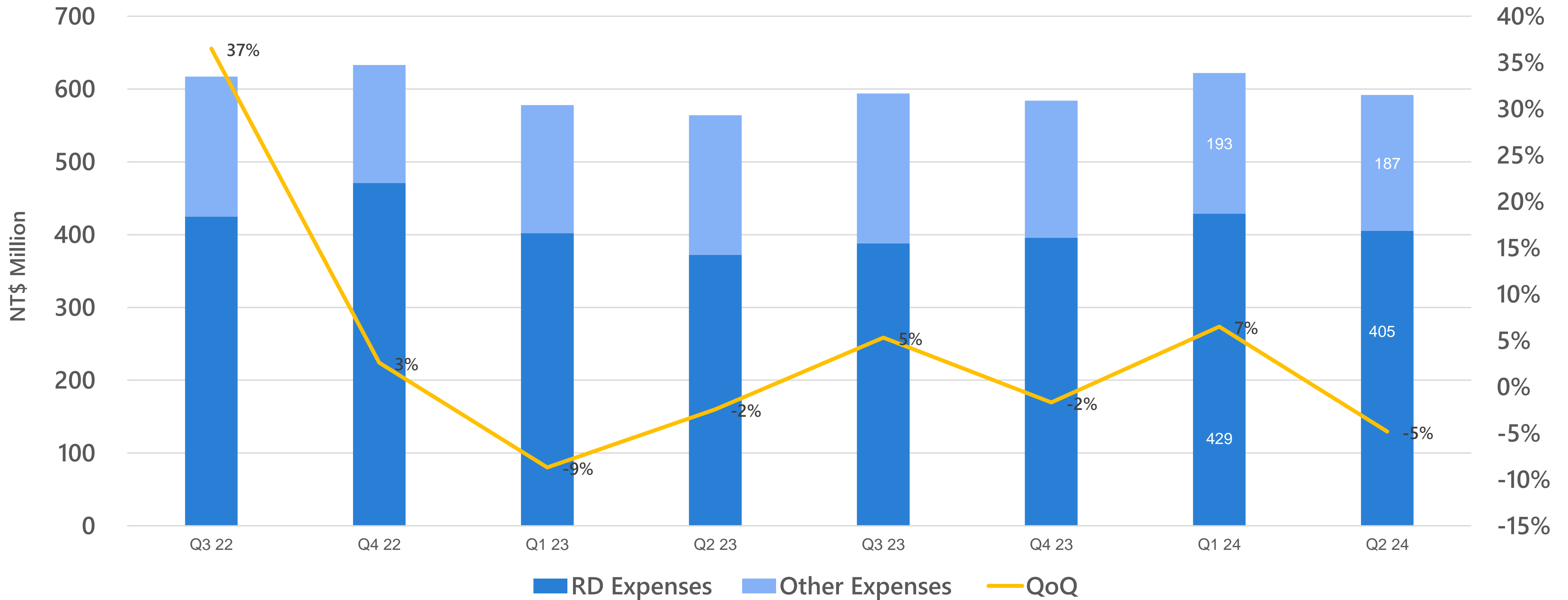
ir@egistec.com

2024.08.20

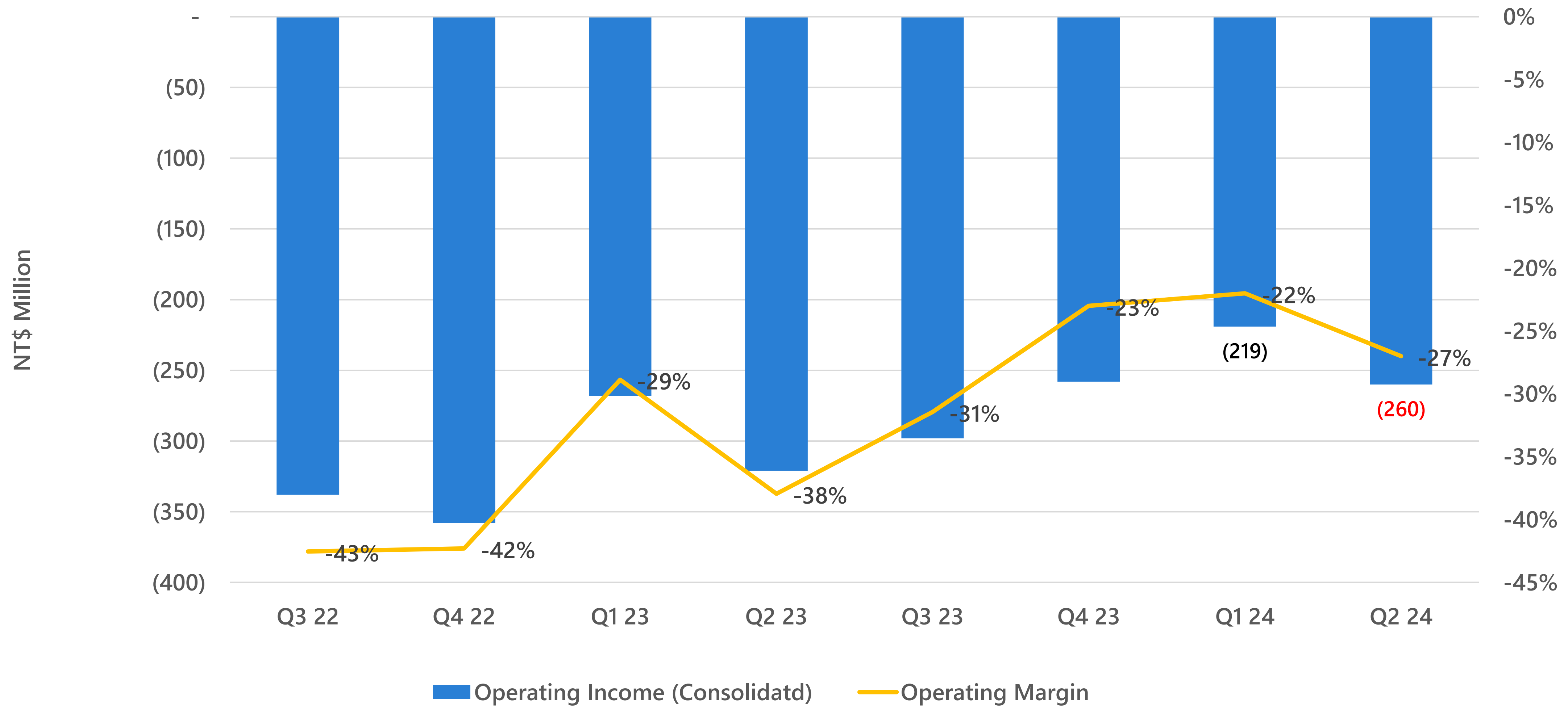
Revenue and GM trend



Operating Expenses

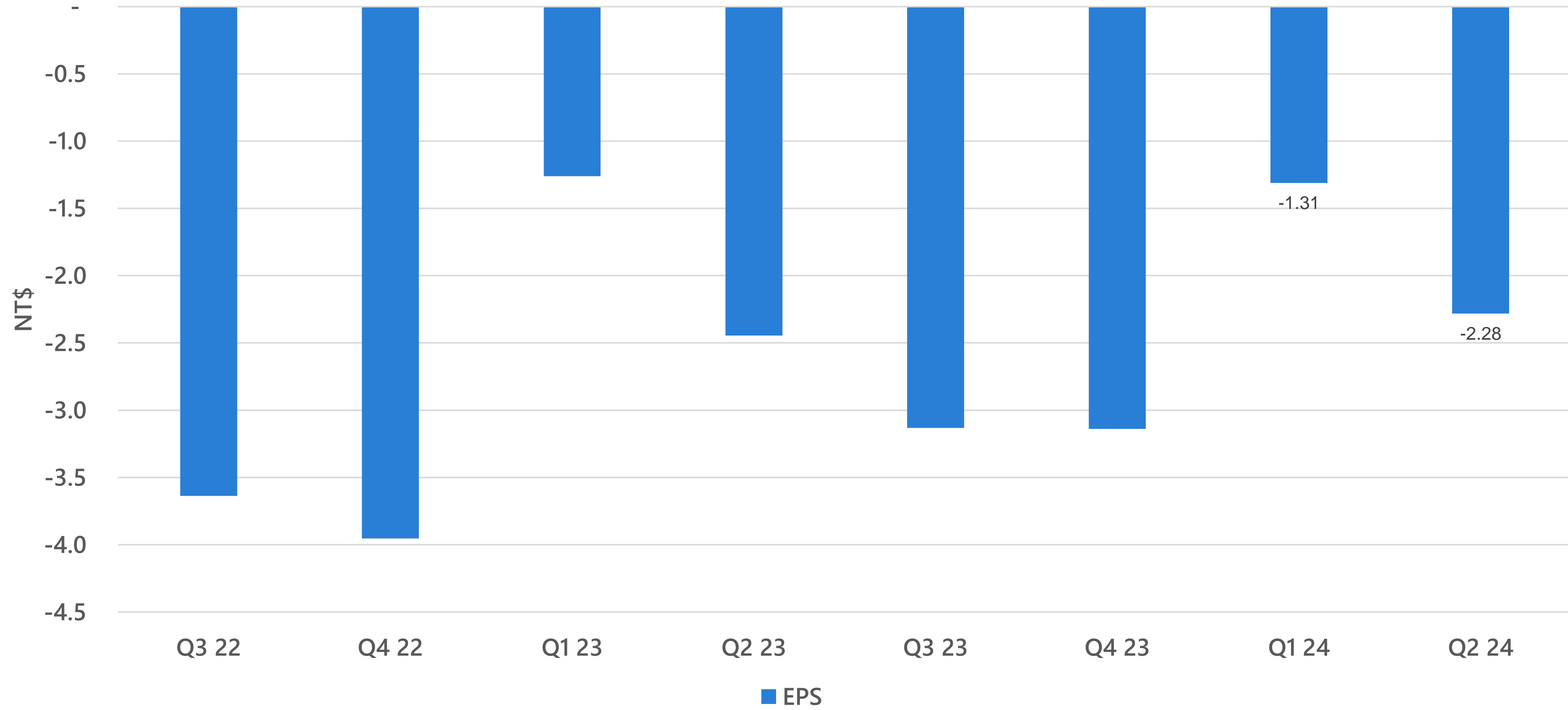


Operating Income



| © 2023 Egis Technology Inc.
CONFIDENTIAL

EPS



Income Statement Q2 2024 vs. Q2 2023

Unit: NT$ Thousands	Q2 2024	Q2 2023	Growth Rate
Net Sales	951,047	845,635	12%
COGS	618,811	602,313	
Gross Profit	332,236	243,322	37%
Gross Margin	35%	29%	
Operating Expense	591,831	564,184	
Operating Income	(259,595)	(320,862)	19%
Operating Margin	-27%	-38%	
Non-operating Income and Expense	43,137	81,902	
Income before Tax	(216,458)	(238,960)	
Income Tax Expense (Income)	(9,630)	(61,447)	
Income after Tax	(206,828)	(177,513)	
Minority Interest	(37,480)	(2,004)	
Parent Net Income (Loss)	(169,348)	(175,509)	4%
Net Margin	-17.8%	-20.8%	
EPS (NT$)	(2.28)	(2.44)	

Balance Sheet (1)

Unit: NT$ Thousands	Q2 2024	Q2 2023
Cash and cash equivalents	2,219,420	1,429,202
Financials assets at fair value through P&L	660,035	997,233
Notes and accounts receivable, net	461,246	633,939
Inventories	700,269	1,287,390
other current assets	1,063,148	1,392,472
Total current assets	5,104,118	5,740,236
Non-current assets		
Financials assets at fair value through P&L	670,106	1,026,458
Financials assets at fair value through OCI	2,425,826	2,005,289
Investments accounted for using equity method	1,336,268	1,537,692
other non-current assets	3,199,684	2,054,915
Total non-current assets	7,631,884	6,624,354
Total Assets	**12,736,002**	**12,364,590**

Balance Sheet (2)

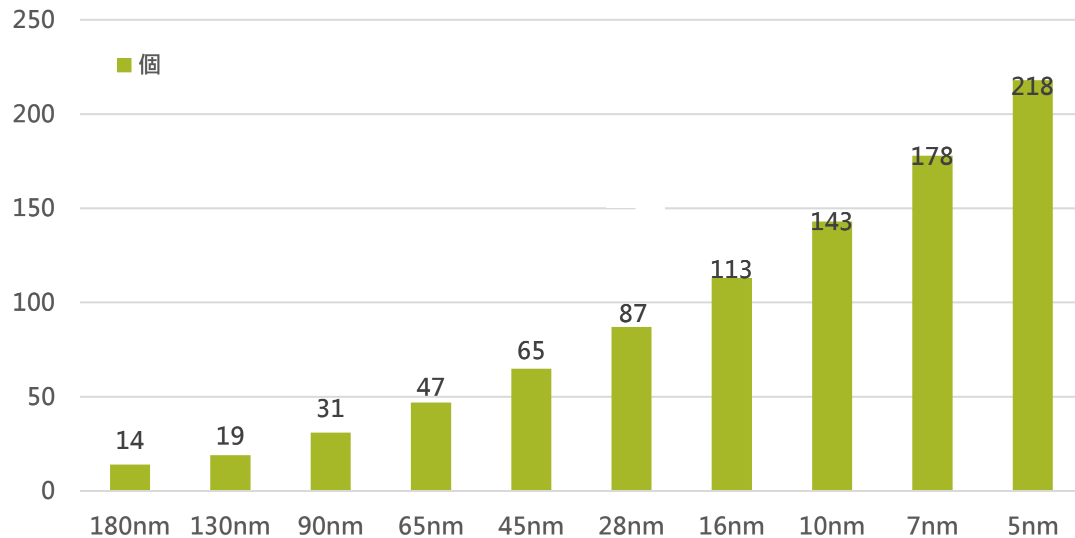
Unit: NT$ Thousands	Q2 2024	Q2 2023
Current liabilities		
Short-term borrowings	1,234,000	1,317,500
Notes and accounts payable	353,442	282,072
Long-term liabilities, current portion	437,200	368,036
other current liabilities	1,413,818	956,162
Total current liabilities	3,438,460	2,923,770
Non-Current liabilities		
Long-term debt	688,464	965,664
other non-current liabilities	836,313	341,431
Total non-ccurrent liabilities	1,524,777	1,307,095
Total Liabilities	**4,963,237**	**4,230,865**
Total Equity	**7,772,765**	**8,133,725**

Egis Third Wave Transformation
AI HPC Server

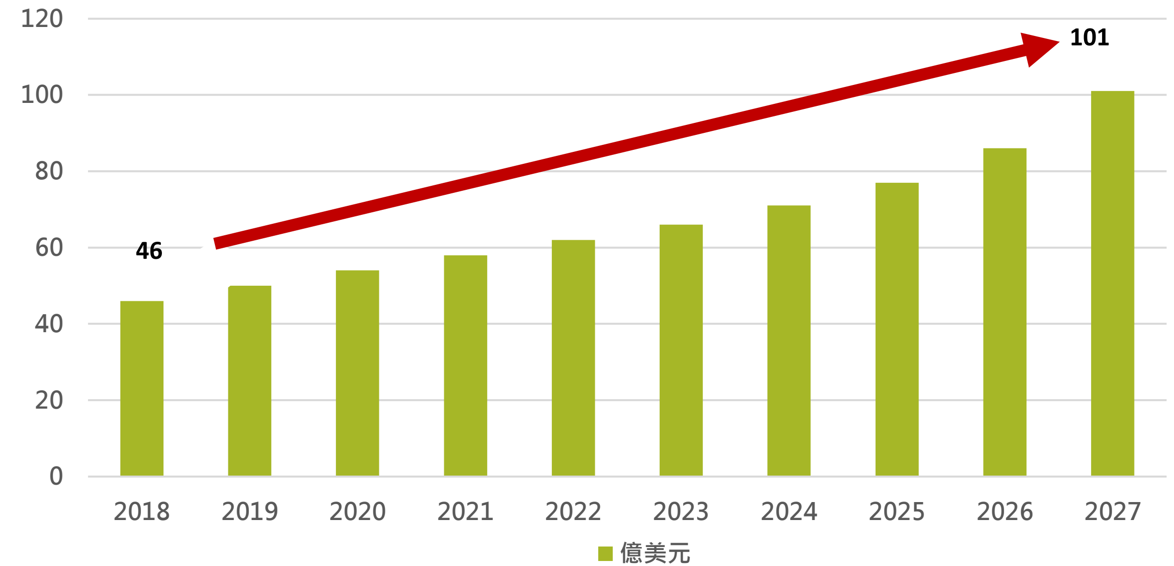
082024 神盾法說會

The Importance of IP for Advanced Processes

More Advanced Process needs more IPs.

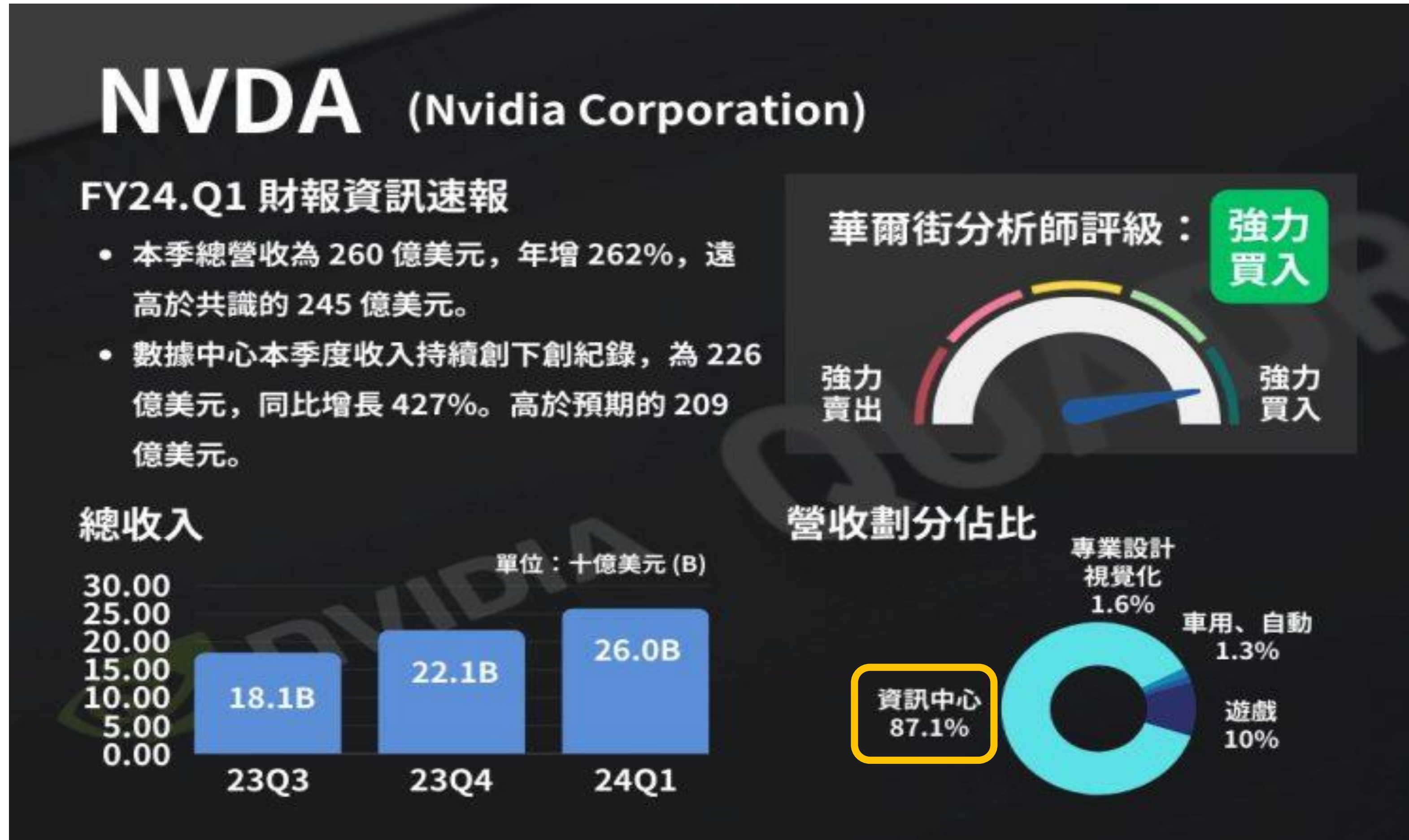


Global Semiconductor IP Market Size



NVDIA Revenue

2024 Q1 NVDIA 淨利相當於全球前十大 IC 設計公司淨利的40%



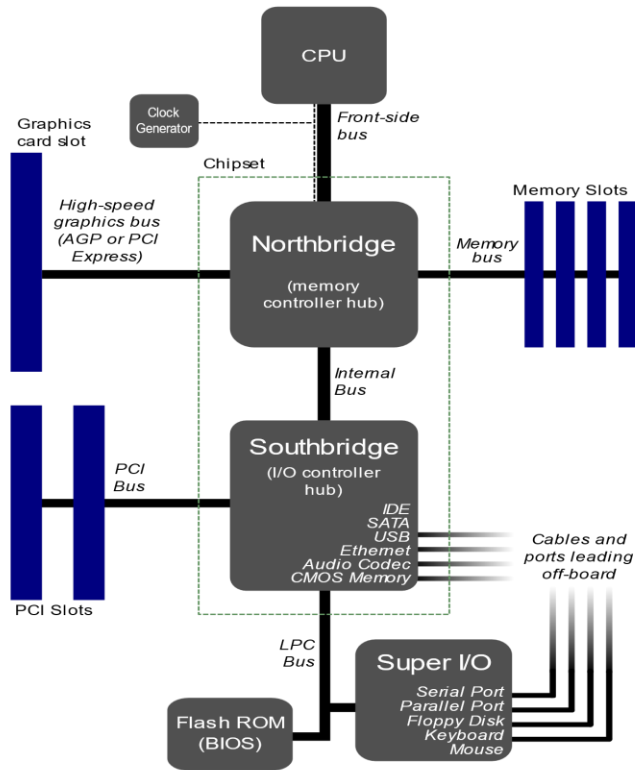
Future：HPC

- TSMC 2024 Q2 Revenue Growth Rate：
  1. HPC from 46% to 52%
  2. Mobile phone from 38% to 33%
  3. Advanced process total 85%

- TSMC 2024 AI Accelerator Revenue Growth rate 2.5x

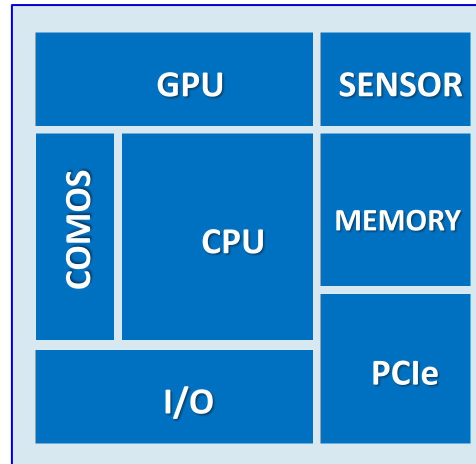
The Evolution of Chips

CPU + Chipset



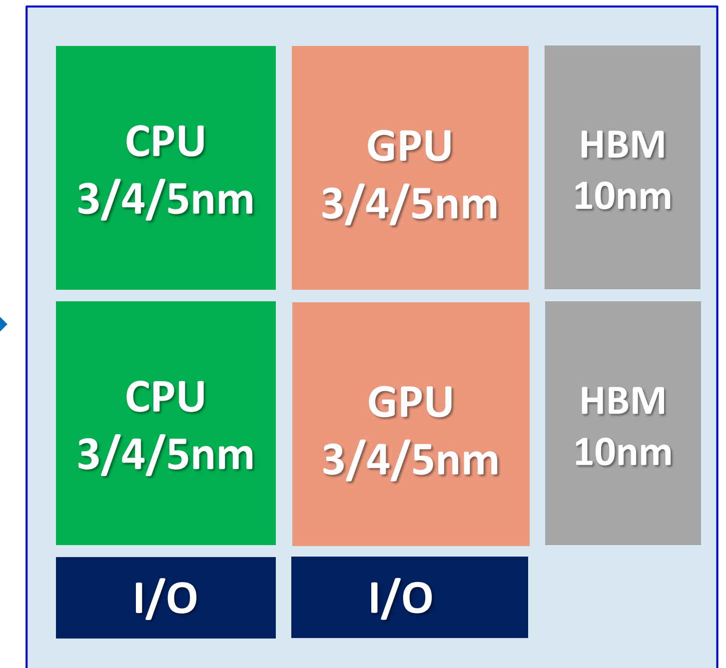
SoC

- Manufacture by the same fab and same process



Chiplet

- Manufacture by the different fab and different process



Moore's Law

More than Moore

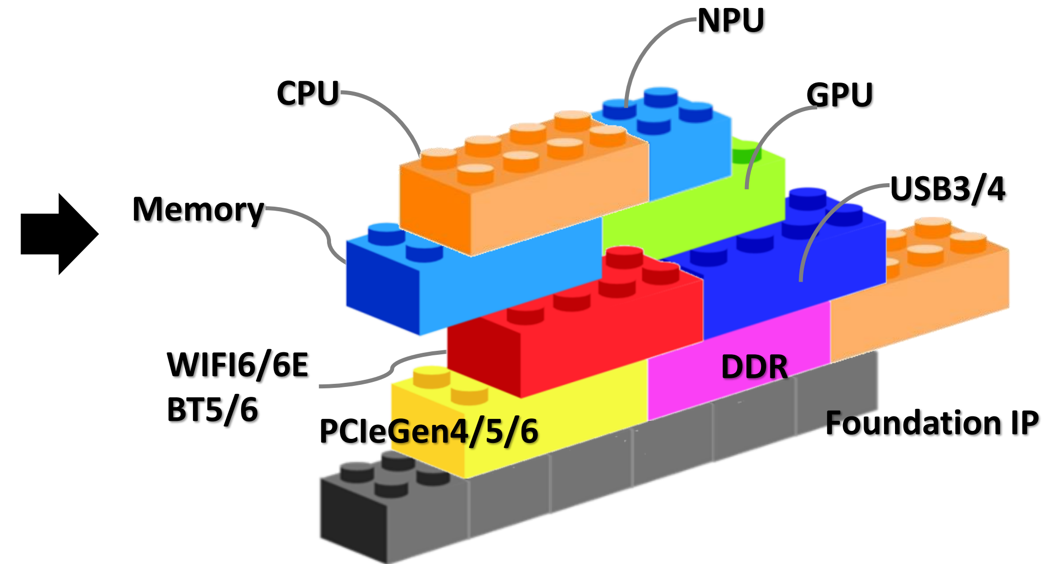
Blueprint：IP is the building block of Chip

Functional IP

CPU | GPU | NPU
WIFI6/6E/7 | BT5/6 | UWB
LVDS | HDMI | DP/eDP
MIPI A-PHY | MIPI C/D-PHY | SLVS
USB3/4/4v2 | PCIeGen 4/5/6 | MIPI M-PHY
UCIe (D2D) | DDR3/4/5 Combo | ONFI

Foundation IP –

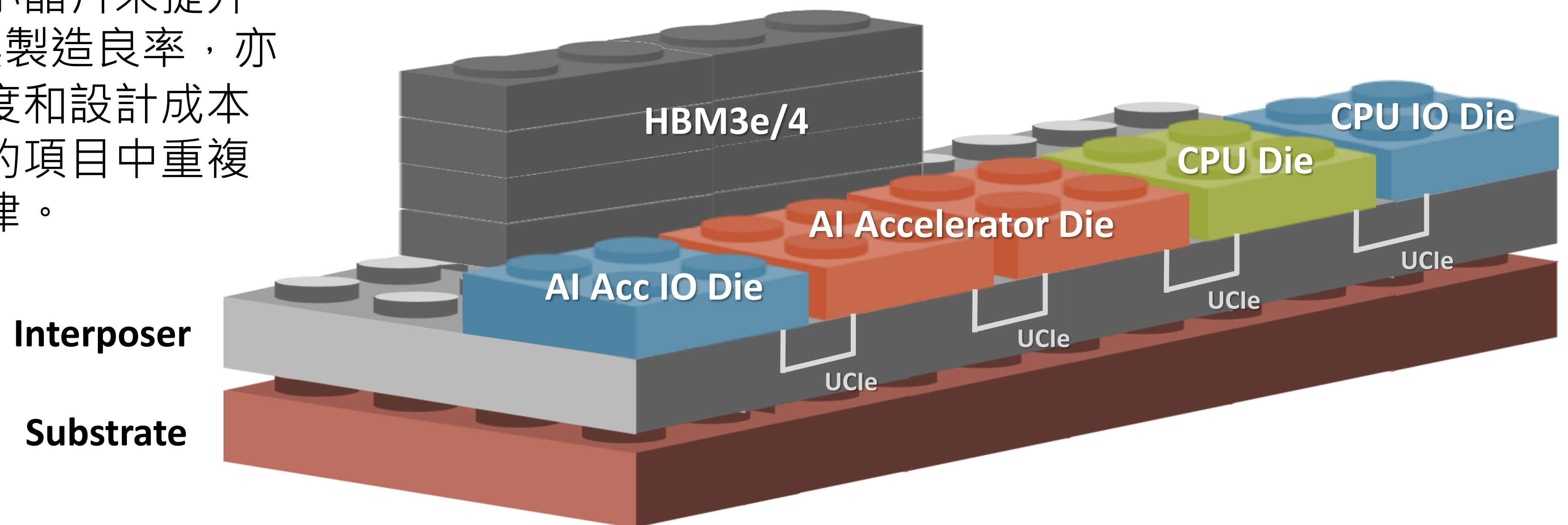
Standard Cell | Memory Compiler | IO



Chiplet 是 IC 設計架構的典範轉移

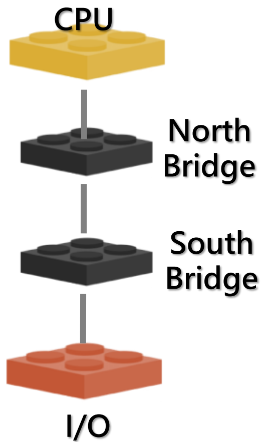
- Chiplet 主要是將大晶片化整為零，單顆晶片本質上是 IP 硬件化，透過 UCIe 連接及先進封裝技術 (CoWoS) 將多顆硬件化的 IP 混合搭配「樂高式」堆疊組件於單一基板上。

- Chiplet 技術可以整合面積相對小、製造良率相對高且可合併不同工藝節點製造的各種小晶片來提升晶片性能 (PPA) 及其製造良率，亦有降低設計的複雜度和設計成本的優勢，並在不同的項目中重複使用，延續摩爾定律。



Chip/Chiplet is stacked (Lego) by IP/Harden IP

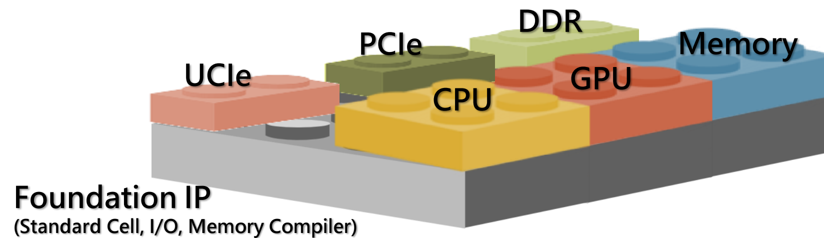
CPU + Chipset



SoC

Single Die

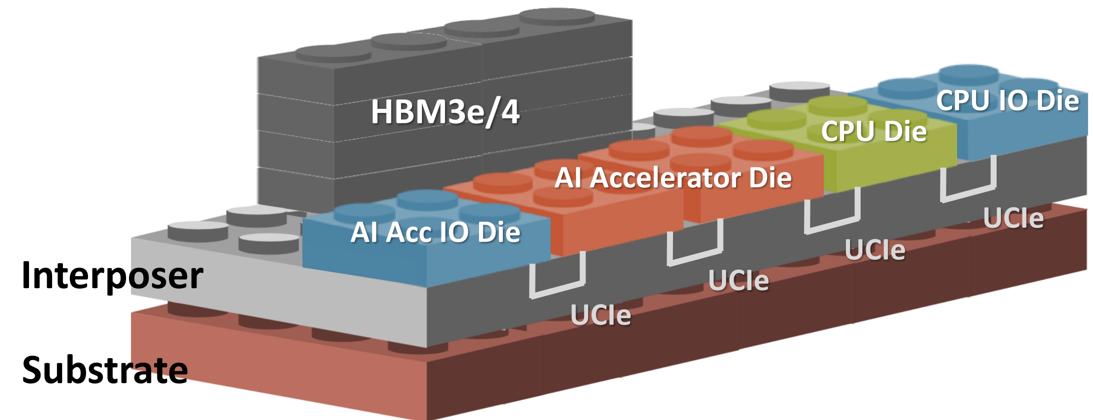
- IP is the building block of Chip
- Manufacture by the same fab and same process



Chiplet

Multi-Die

- Multiple Die (harden IPs) are stacked and integrated on the interposer through UCIe connection and advanced packaging technology (CoWoS)
- Manufacture by the different fab and different process



Moore's Law → More than Moore

Egis | © 2023 Egis Technology Inc. CONFIDENTIAL

Foundation of Chiplet

- UCIe (Universal Chiplet Interconnect Express)
- CoWoS

  CoWoS-S：3.3x reticle (858 x 3.3 = 2831.4)

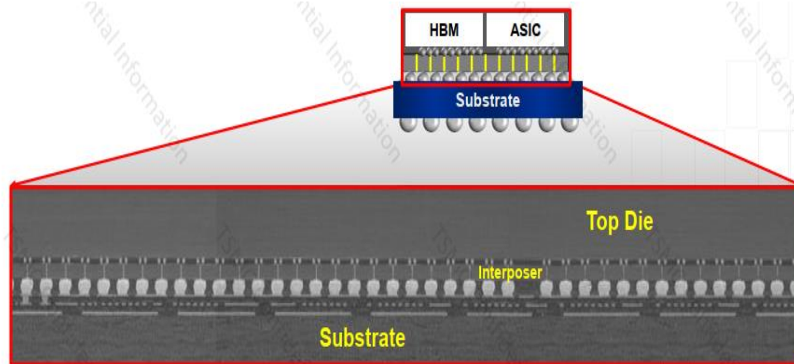
  CoWoS-R：4x reticle (858 x 4 = 3432)

  CoWoS-L：6x reticle (858 x 6 = 5148)

Advanced Package - CoWoS

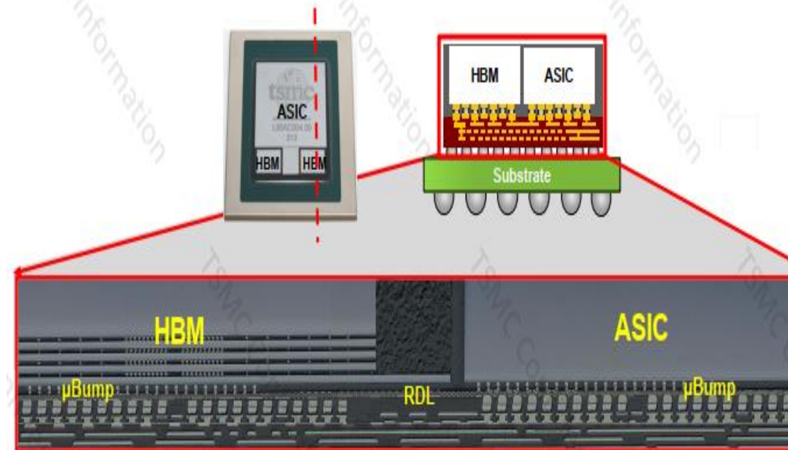
CoWoS-S

3.3x reticle (858 x 3.3 = 2831.4)



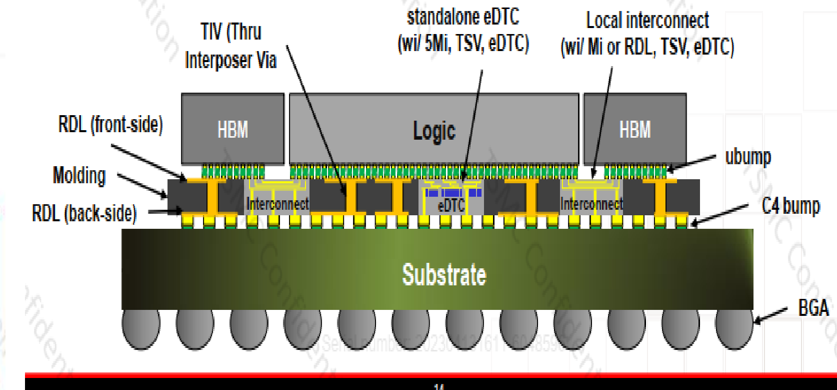
CoWoS-R

4x reticle (858 x 4 = 3432)



CoWoS-L

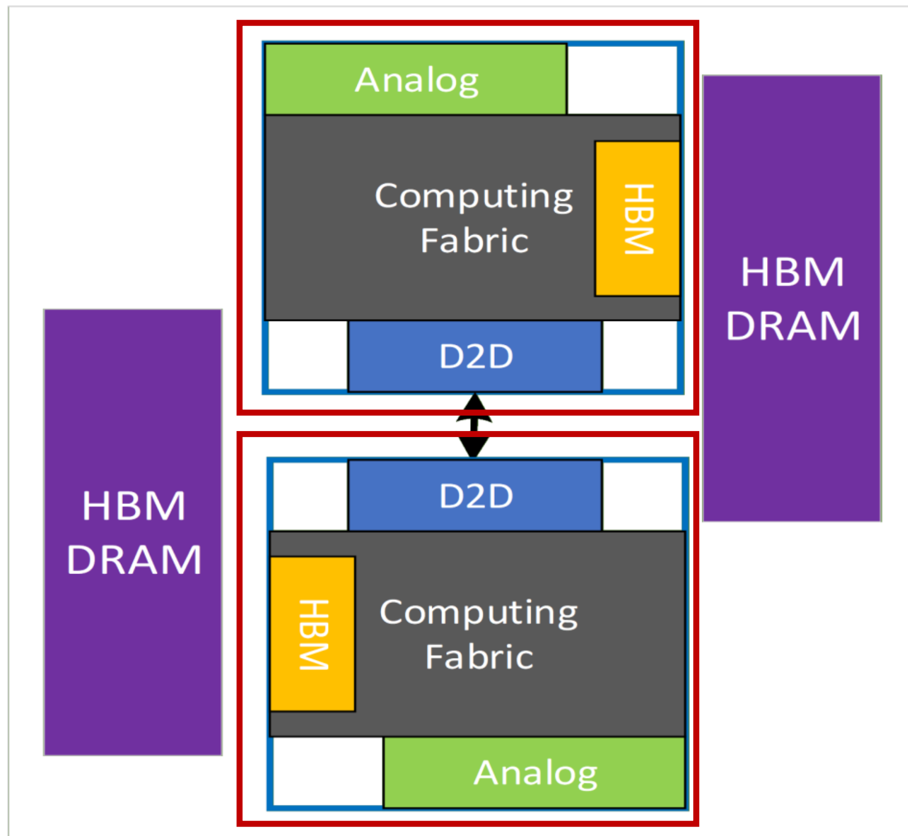
6x reticle (858 x 6 = 5148)



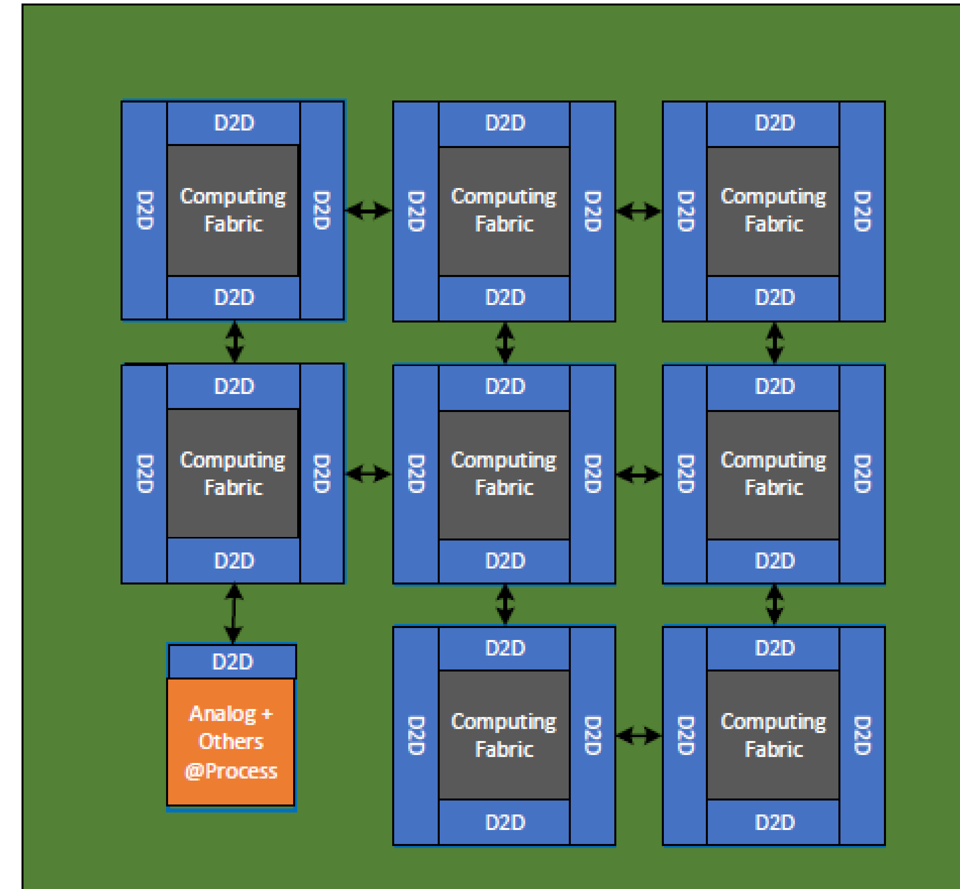
*reticle (1x=858 (26 x 33))

UCIe Advanced Package - CoWoS

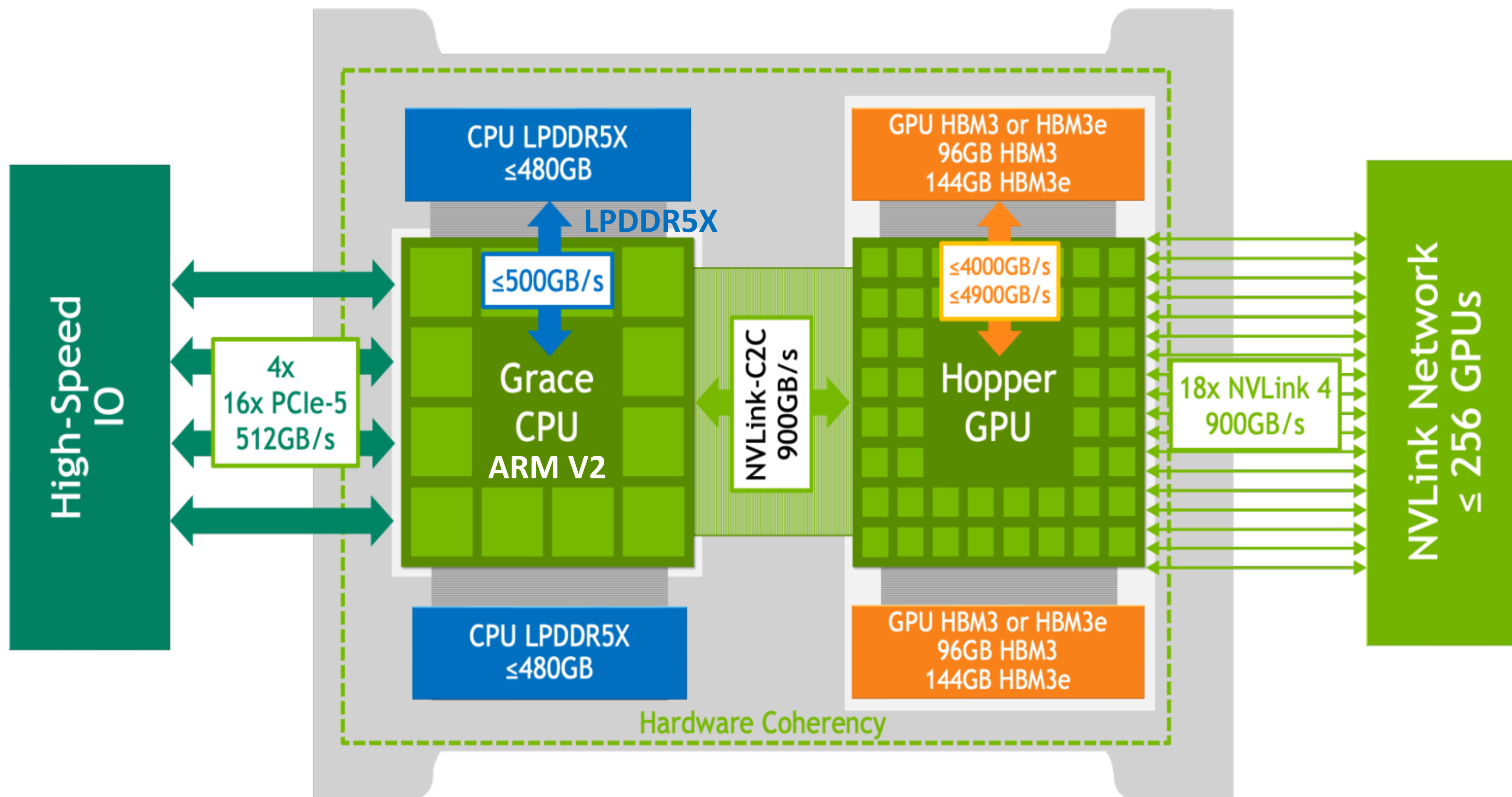
- 5/4nm (8 channel, 48Tx/48Rx per channel)
  - 12.3Tbps data rate @16G per bit per PHY
  - Latency 3~4ns



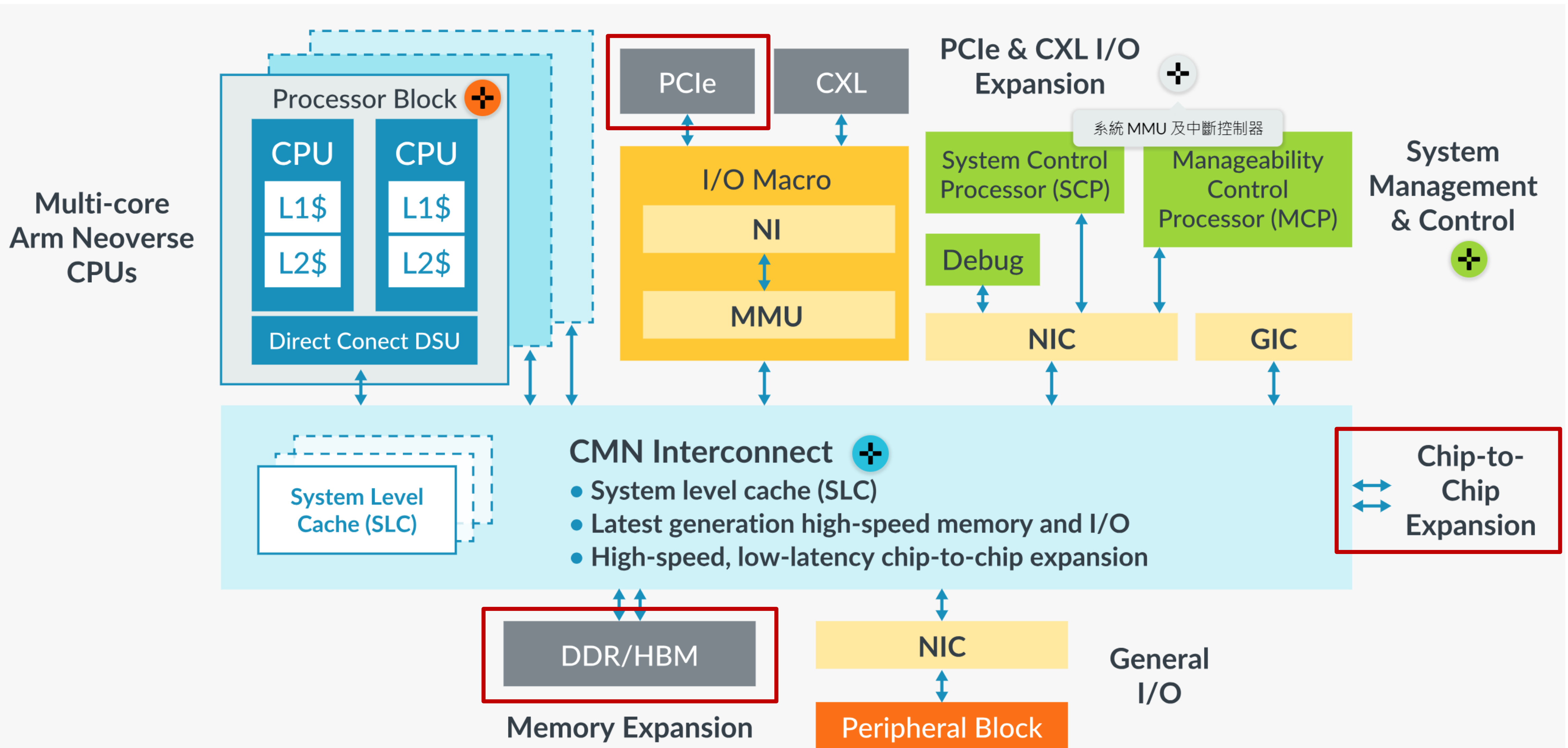
- 3nm (8 channel, 64Tx/64Rx per channel)
  - 16.38Tbps data rate @16G per bit per PHY
  - Latency 3~4ns



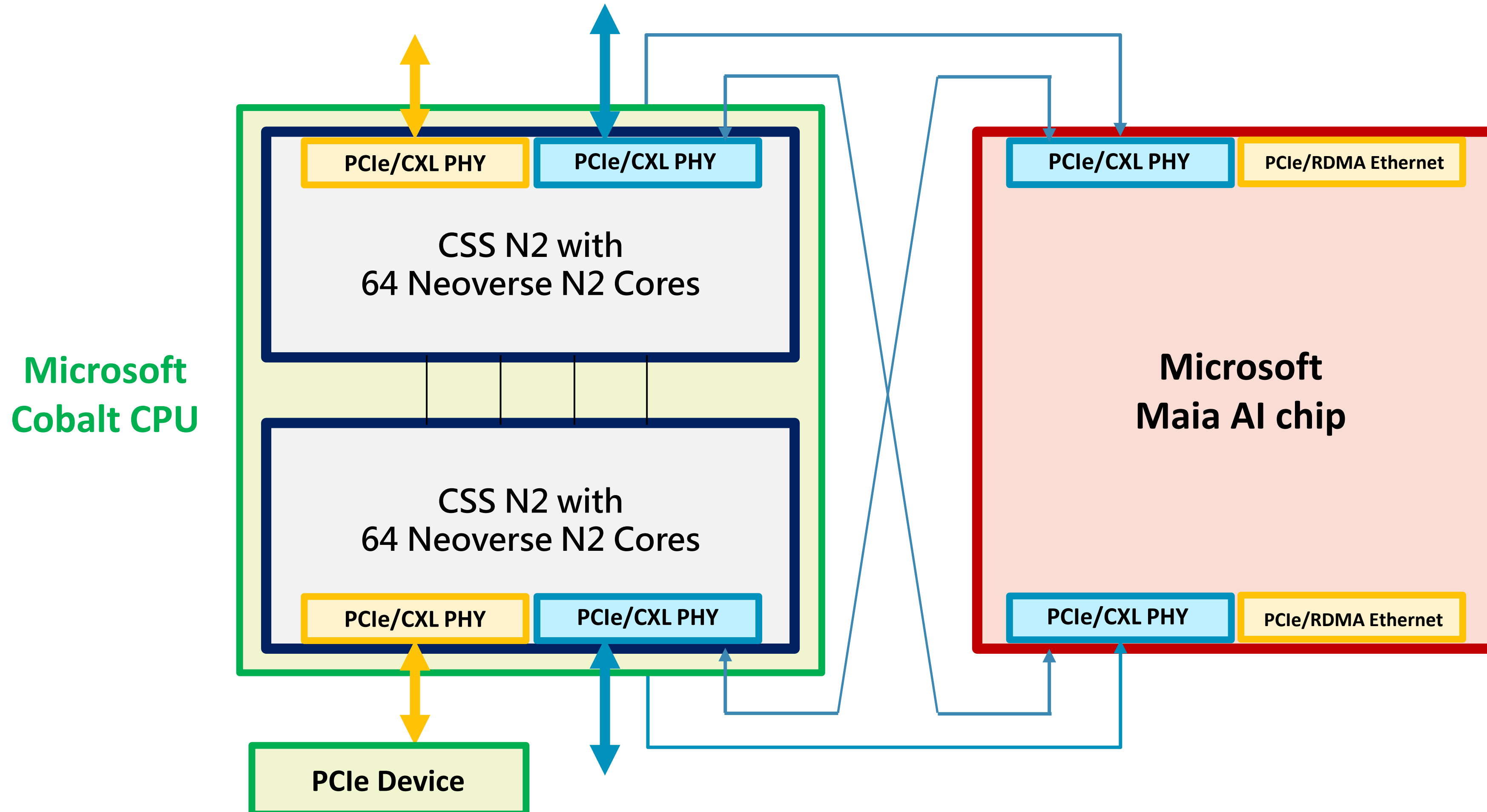
AI HPC Server Chiplet Architecture



Egis Group IP & ARM CSS

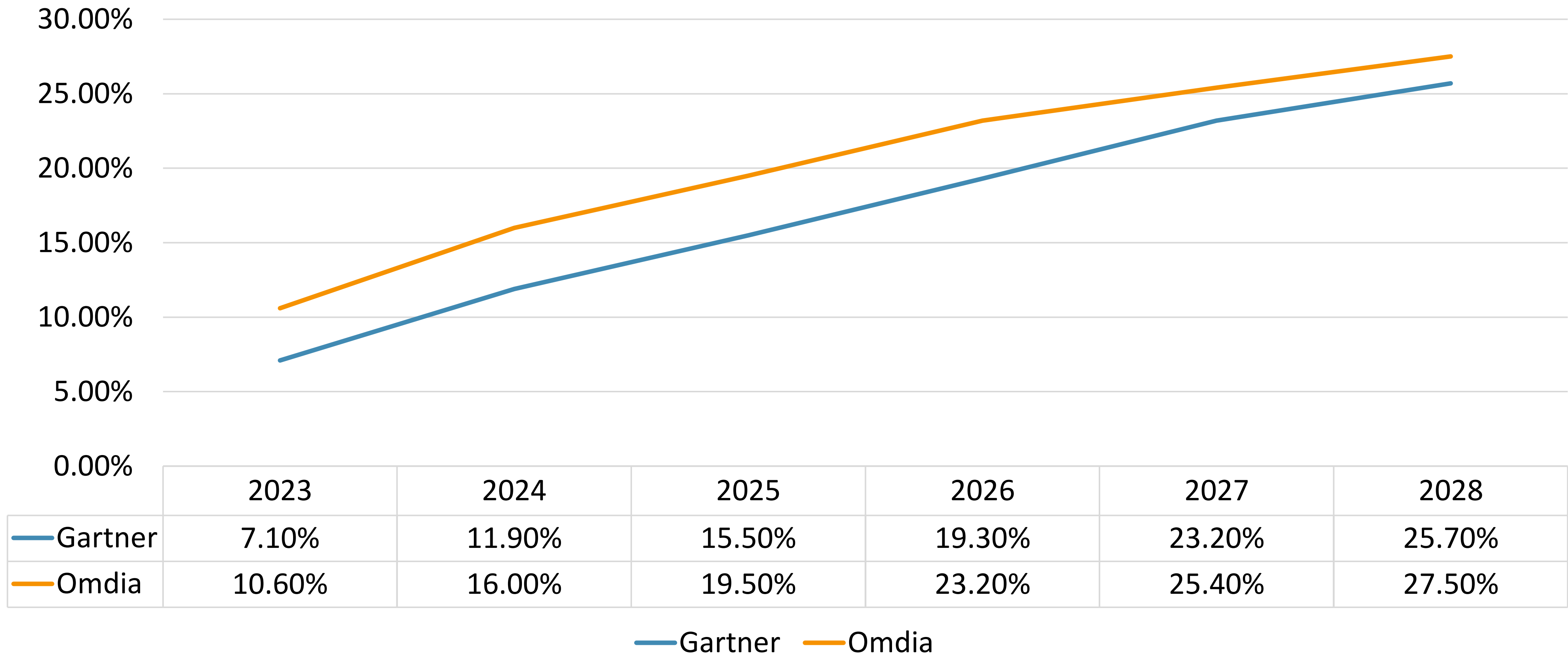


AI HPC Server Chiplet Architecture



ARM Server Market Share Momentum

Analysts Forecast：Arm targeted to hit 16%-20% server market share by 2025



	2023	2024	2025	2026	2027	2028
Gartner	7.10%	11.90%	15.50%	19.30%	23.20%	25.70%
Omdia	10.60%	16.00%	19.50%	23.20%	25.40%	27.50%

Global ARM-Based Servers Market

TABLE – GLOBAL ARM-BASED SERVERS MARKET, BY APPLICATION, 2022-2031 (USD MILLION)											
Application	**2022**	**2023**	**2024**	**2025**	**2026**	**2027**	**2028**	**2029**	**2030**	**2031**	**CAGR (2024-31)**
Data Centers	2342.8	2621.2	2966.6	3377.6	3866.2	4453.0	5151.1	5989.9	6997.0	8214.9	**15.66%**
Cloud Computing	1007.7	1097.7	1198.6	1313.8	1444.8	1595.0	1765.5	1960.7	2183.7	2439.6	**10.69%**
HPC	831.9	917.0	1013.7	1125.6	1254.9	1405.4	1579.1	1781.4	2016.4	2291.1	**12.36%**
Web Hosting	586.9	643.3	707.0	780.3	864.5	961.8	1073.4	1202.3	1351.0	1523.3	**11.59%**
Enterprise IT	520.0	565.2	615.9	673.7	739.4	814.6	899.9	997.3	1108.4	1235.6	**10.46%**
Telecommunications	506.1	556.2	613.1	678.7	754.2	841.9	942.7	1059.7	1195.0	1352.6	**11.97%**
Retail/ E-commerce	397.6	436.1	484.9	541.8	608.0	685.7	776.1	882.1	1006.3	1152.6	**13.17%**
Others	1108.5	1185.1	1277.6	1381.8	1498.9	1631.2	1779.1	1945.8	2132.9	2343.8	**9.06%**
Total	**7301.5**	**8021.8**	**8877.3**	**9873.3**	**11031.0**	**12388.7**	**13966.7**	**15819.2**	**17990.6**	**20553.5**	**12.74%**

©Exactitude Consultancy

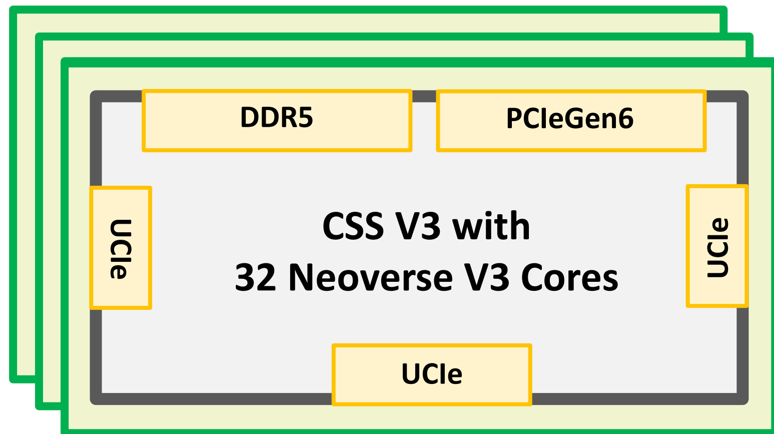
Egis | © 2023 Egis Technology Inc.

CONFIDENTIAL

CPU Chip - Roadmap

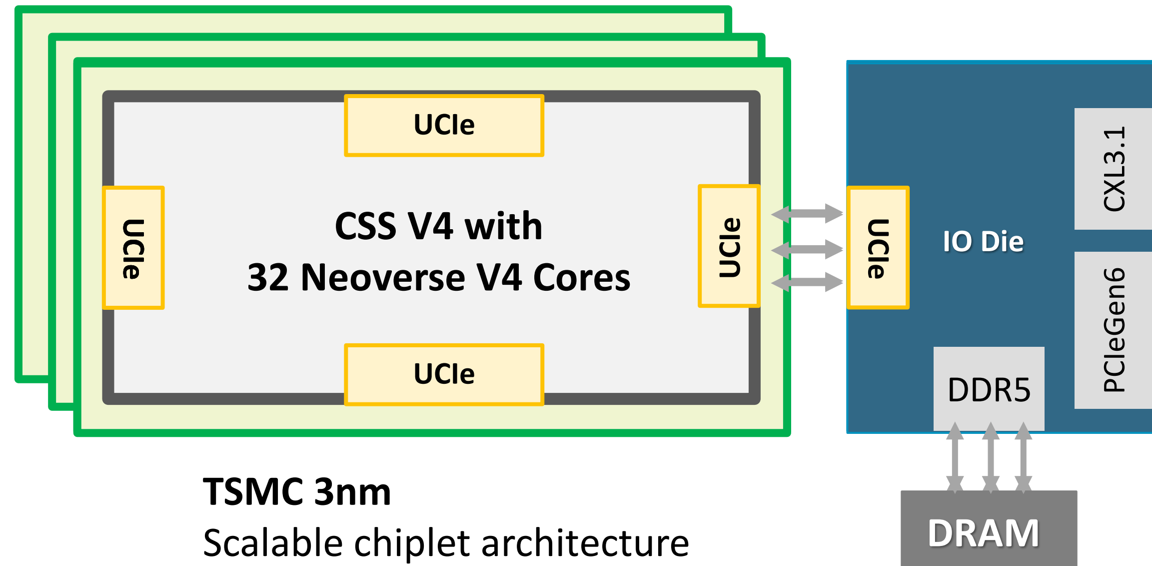
- **The World's first CSS V3 AI HPC Server CPU Chip**

Mobius100 CPU
2025 Q4 TO



TSMC 4nm
Scalable chiplet architecture
UCIe up to 20Gbps

Mobius200 CPU
2026 Q4 TO

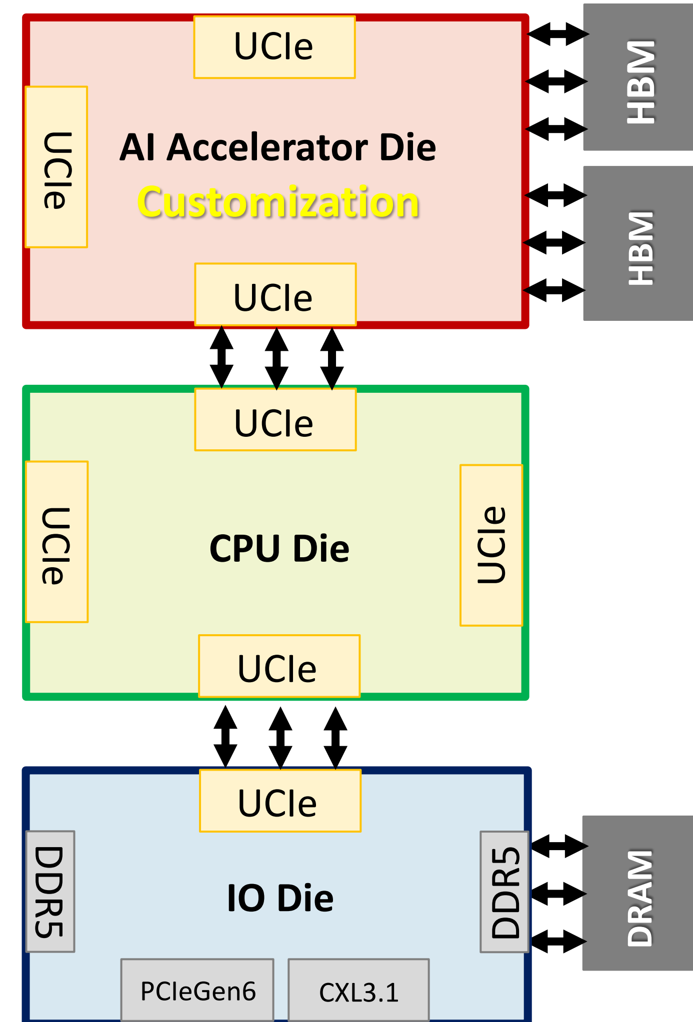


TSMC 3nm
Scalable chiplet architecture
UCIe up to 32Gbps
***Connect with IO Die**

© 2023 Egis Technology Inc. CONFIDENTIAL

Business Strategy & Core Competency

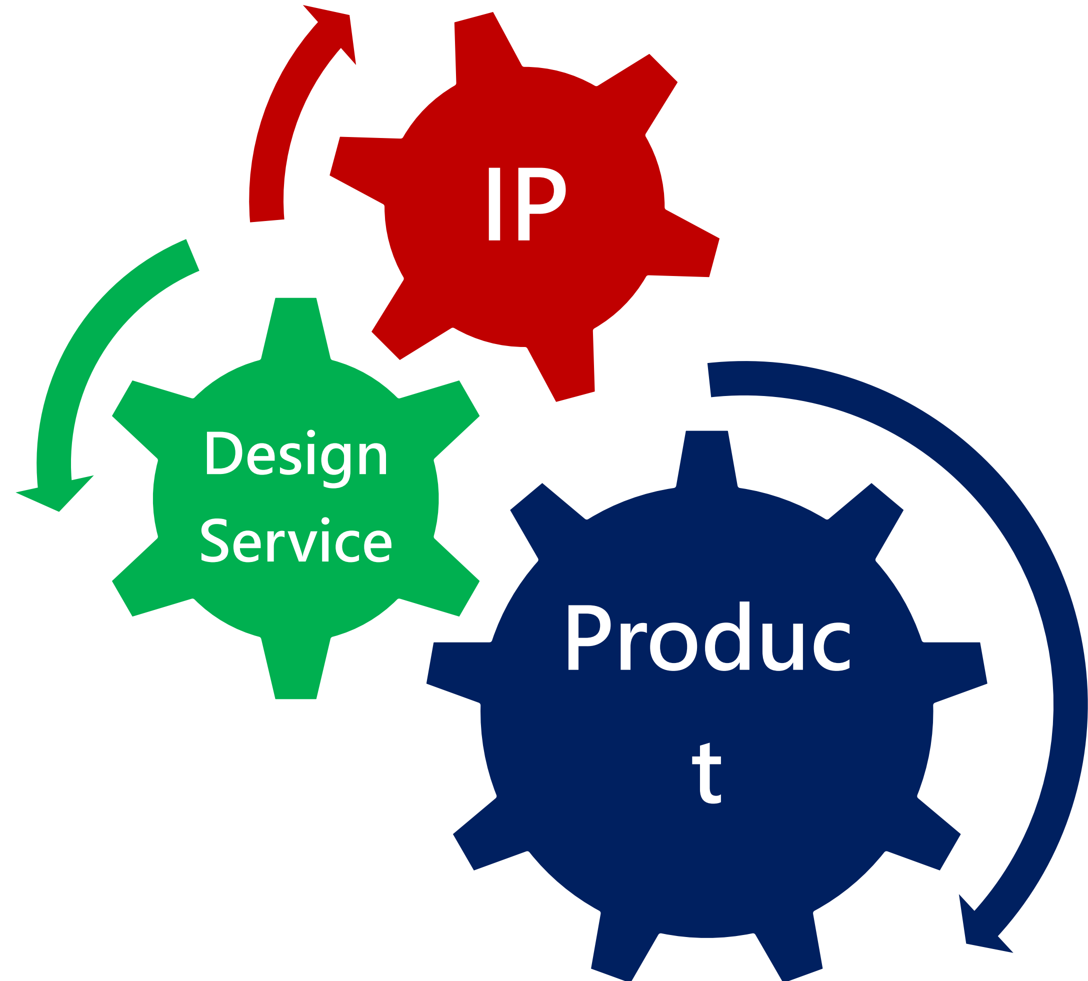
- IP：UCIe (D2D), DDR5, PCIeGen6
- ASIC Design Service：
  - ARM CSS V3 (4nm)
  - AI Accelerator Die Customization
  - CoWoS Turnkey Solution
  - HBM Base Die Design Service
- Chip：CPU chip, I/O chip, AI Accelerator chip



© 2023 Egis Technology Inc. CONFIDENTIAL

神盾集團成長策略與動能

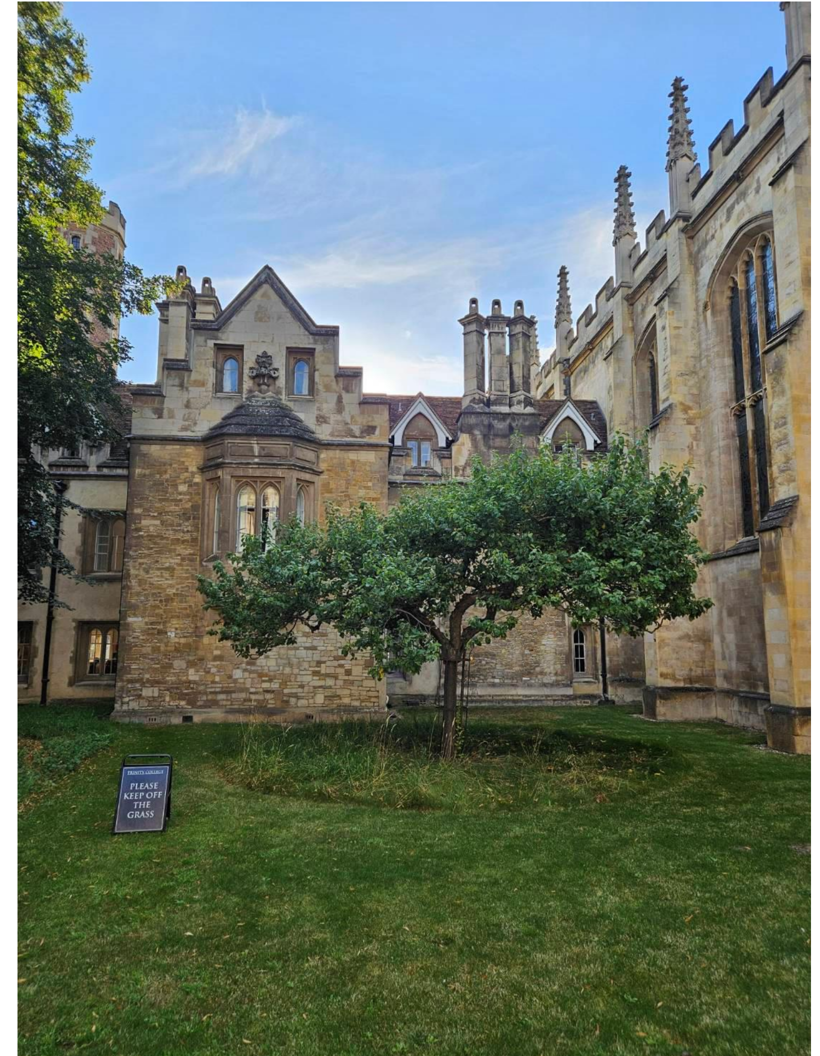
- 2025: IP, Design Service
- 2026: IP, Design Service, IO Chip
- 2027: IP, Design Service, IO Chip,
  ARM based CPU Chip



ARM Future Insight

- Multi-die is everywhere
- Advanced Package (CoWoS)
- AI

Go with Winner



If I have seen further than others, it is by standing on the shoulders of Giants.

and Go further on the way of Success

1000101
1000111
100
1001
1010011

Egis